IN THE CLAIMS

Claims 1-8 are currently pending and stand as follows:

1. (Previously Presented) A processor comprising:

a register file including a plurality of registers assigned with register numbers, each of the registers storing operand data;

a plurality of operation pipes, each operation pipe for executing in parallel one kind of operation on a plurality of the operand data;

a decoder for decoding a register designating field of an instruction code, said register designating field having a register number stored therewith, said decoder further for generating signals designating register numbers based on the register number of the register designating field, said designated register numbers being consecutive with the register number of the register designating field; and

a control circuit for sending operand data stored in the registers corresponding to the designated register numbers to at least one of the operation pipes such that said at least one of the operation pipes executes in parallel the one kind of operation associated therewith on the operand data sent from the corresponding designated registers.

2. (Previously Presented) A processor comprising:

a register file including a plurality of registers assigned with register numbers;

a plurality of operation pipes, each operation pipe for executing in parallel one kind of operation on a plurality of operand data so as to generate operation result data;

a decoder for decoding a register designating field of an instruction code, said register designating field having a register number stored therewith, said decoder further for generating signals designating register numbers based on and consecutive with the register number of the register designating field, and the registers corresponding to the designated register numbers being designated for storing the operation result data; and

a control circuit for sending the operation result data from at least one of the operation pipes to the corresponding designated registers.

3. (Previously Presented) A processor comprising:

a register file including a plurality of registers assigned with register numbers, each of the registers for storing at least one of operand data and operation result data;

a plurality of operation pipes, each operation pipe for executing in parallel one kind of operation on a plurality of the operand data so as to generate the operation result data;

a first decoder for decoding a first register designating field of an instruction code, said first register designating field having a first register number stored therewith, said first decoder further for generating signals designating source register numbers based on and consecutive with the first register number;

a second decoder for decoding a second register designating field of the instruction code, said second register designating field having a second register number stored therewith, said second decoder further for generating signals designating result register numbers based on and consecutive with the second register number; and

a control circuit for sending the operand data stored in source registers corresponding to the designated source register numbers to at least one of the operation pipes such that said at least one of the operation pipes executes in parallel the one kind of operation associated therewith on the operand data and for sending the operation result data obtained from the at least one operation pipe to result registers corresponding to the designated result register numbers.

4. (Previously Presented) The processor according to Claim 3, wherein the plurality of registers are divided into a plurality of banks, and by reading or writing data from the plurality of banks, the number of ports of reading or writing the data of respective banks is restricted to be equal to or smaller than a number of the register designating fields so as to restrain an increase in a circuit scale caused by reading or writing the data by a number of times larger than the number of the register designating fields contained in the instruction code.

5. (Previously Presented) The processor according to Claim 1, wherein the number of the plurality of registers is limited to the n-th power of 2 where n is a natural number, so as to reduce register selecting circuits.

6. (Previously Presented) The processor according to Claim 3, wherein a data pack operation, which deals with a number of the data read from the source registers larger than a number of the data written to the result registers, data read from the source registers are larger in a number than a number of the register designating fields contained in the instruction code so as to eliminate invalid portions in the result registers.

7. (Previously Presented) The processor according to Claim 3, wherein a data unpack operation, which deals with a number of the data written to the result registers larger than a number of the data read from the source registers, a number of data written in parallel to the result registers is larger than a number of the register designating fields contained in the instruction code so as to avoid data writing a plurality of times.

8. (Previously Presented) The processor according to Claim 3, wherein an operation of outputting the data having a data width wider than a width of input data such that a number of data larger than a number of the write register designating fields contained in the instruction code can be written to the results registers so as to eliminate invalid portions in the input data and avoid mounting a special register having a wider data width.